Notice of Allowability	Application No.	Applicant(s)	
	10/783,112	TAYLER ET AL.	
	Examiner	Art Unit	
	Elmira Mehrmanesh	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *4/28/07*.

2. ☒ The allowed claim(s) is/are *1-33*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

This action is in response to an Appeal Brief filed on April 28, 2007 for the application of Tayler et al., for a "Timeout event trigger generation" filed February 20, 2004.

Claims 1-33 are allowed.

Response to Arguments

Applicant's arguments see Appeal Brief filed on April 28, 2007, with respect to claims 1-33 have been fully considered and are persuasive. The rejection of claims 1-33 has been withdrawn.

Reasons for Allowance

The following is an examiner's statement of reasons for allowance:

After a complete search of all the relevant prior art the examiner has determined the claims are in condition for allowance. The following limitations when viewed in combination with the remainder of the claim as a whole, place this application in condition for allowance.

As per claims 1, 10, 11, 20, and 29, the Examiner finds the novel and non-obvious feature of this claim, when read as a whole to be an overflow generator to generate a *plurality of overflow signals having a plurality of periods* and generating a first timeout event trigger signal based on the plurality of overflow signals and a first one of the plurality of selection values.

The above claims were rejected with the prior art Bailey et al. (U.S. Patent No. 5,012,435). Bailey's figure 8 shows a counter 530 connected by a line 542 to a clock 540. The output of the counter on line 532 is provided to registers 510A

510B and 510C together with comparator circuits 550A, 550B and 550C, which provide outputs to the timeout logic 560 via lines 552A, 552B and 552C. These signals are then used together with the output on line 585 from the timeout logic 560 to determine that a timeout condition has occurred (col. 7, lines 15-35). Bailey's figure 5 shows time periods generated by the clock (Fig. 8, element 540).

Bailey's counter (Fig. 8, element 530) produces signals in plurality of periods. Bailey's counter 530 is similar to the present application's counter (Fig. 3, element 302). Both counters generate signals at multiple clock periods. Bailey's counter 530 generates signal 532 and the present application's counter 302 generates signals 224 a-d as depicted in figure 3.

However the process of generating the overflow signals having a plurality of periods in the present application is not thought by Bailey. Referring to applicant's arguments (see Appeal Brief, page 12), and further in light of figure 3 of the present application, the generation of the overflow signals by the overflow signal generator 220 differs from the Bailey's reference, since Bailey fails to disclose a plurality of signals having a plurality of periods. Therefore the above claims overcome the Bailey reference.

As per claim 21, the Examiner finds the novel and non-obvious feature of this claim, when read as a whole to be a multiplexer comprising a plurality of data inputs to receive a plurality of overflow signals, a selection input to receive a selection signal, and an output to provide one of the plurality of overflow signals

selected by the selection signal; a one-bit counter comprising a data input coupled to the output of the multiplexer, a reset input, and a data output to provide a one-bit count signal; and an AND gate having a first input coupled to the data output of the one-bit counter, a second input coupled to the output of the multiplexer, and an output to provide a first timeout event trigger signal.

Bailey's figure 8 shows a counter 530 connected by a line 542 to a clock 540. The output of the counter on line 532 is provided to registers 510A 510B and 510C together with comparator circuits 550A, 550B and 550C, which provide outputs to the timeout logic 560 via lines 552A, 552B and 552C. These signals are then used together with the output on line 585 from the timeout logic 560 to determine that a timeout condition has occurred (col. 7, lines 15-35).

Referring to applicant's arguments (see Appeal Brief, pages 16-17), and further in light of figure 4 of the present application, the generation of the timeout signal differs from the Bailey's reference, since Bailey fails to disclose a multiplexer comprising a plurality of data inputs to receive a plurality of overflow signals and an AND gate having a first input coupled to the data output of the one-bit counter, a second input coupled to the output of the multiplexer, and an output to provide a first timeout event trigger signal. Therefore the above claim overcomes the Bailey reference.

As per claim 23, the Examiner finds the novel and non-obvious feature of this claim, when read as a whole to be receiving a plurality of overflow signals, means for receiving a selection signal, means for selecting one of the plurality of

overflow signals based on the selection signal; counting the number of times the selected one of the plurality of overflow signals has been asserted since a predetermined reset event; and timeout event trigger signal generation means for asserting a timeout event trigger signal when the selected one of the plurality of overflow signals has been asserted twice since the predetermined reset event.

Bailey's figure 8 shows a counter 530 connected by a line 542 to a clock 540. The output of the counter on line 532 is provided to registers 510A 510B and 510C together with comparator circuits 550A, 550B and 550C, which provide outputs to the timeout logic 560 via lines 552A, 552B and 552C. These signals are then used together with the output on line 585 from the timeout logic 560 to determine that a timeout condition has occurred (col. 7, lines 15-35).

Referring to applicant's arguments (see Appeal Brief, page 15), and further in light of figure 4 of the present application, the generation of the timeout signal differs from the Bailey's reference, since Bailey fails to disclose selection means to receive a plurality of overflow signals and a counter for counting the number of times the selected one of the plurality of overflow signals has been asserted and asserting a timeout event trigger signal based on the overflow signals and the counter value. Therefore the above claim overcomes the Bailey reference.

As per claim 25, the Examiner finds the novel and non-obvious feature of this claim, when read as a whole to be a multiplexer comprising a plurality of data inputs to receive a plurality of overflow signals, a selection input to receive a

selection signal, and an output to provide one of the plurality of overflow signals selected by the selection signal; a multi-bit counter comprising a data input coupled to the output of the multiplexer, a reset input, and a plurality of data outputs to provide a multi-bit count signal; a multi-bit comparator having a first plurality of inputs coupled to the plurality of data outputs of the multi-bit counter, a second plurality of inputs to receive a multi-bit control signal, and a data output to provide a comparison signal indicating whether the multi-bit count signal is equal to the multi-bit control signal; and an AND gate having a first input coupled to the data output of the multi-bit comparator, a second input coupled to the output of the multiplexer, and an output to provide a first timeout event trigger signal.

Bailey's figure 8 shows a counter 530 connected by a line 542 to a clock 540. The output of the counter on line 532 is provided to registers 510A 510B and 510C together with comparator circuits 550A, 550B and 550C, which provide outputs to the timeout logic 560 via lines 552A, 552B and 552C. These signals are then used together with the output on line 585 from the timeout logic 560 to determine that a timeout condition has occurred (col. 7, lines 15-35).

Referring to applicant's arguments (see Appeal Brief, pages 16-17), and further in light of figure 4 of the present application, the generation of the timeout signal differs from the Bailey's reference, since Bailey fails to disclose a multiplexer comprising a plurality of data inputs to receive a plurality of overflow signals and an AND gate having a first input coupled to the data output of the one-bit counter, a second input coupled to the output of the multiplexer, and an

output to provide a first timeout event trigger signal. Therefore the above claim overcomes the Bailey reference.

As per claim 27, the Examiner finds the novel and non-obvious feature of this claim, when read as a whole to be means for receiving a plurality of overflow signals, means for receiving a selection signal, means for selecting one of the plurality of overflow signals based on the selection signal, and means for providing as output the selected one of the plurality of overflow signals; counting means for counting the number of times the selected one of the plurality of overflow signals has been asserted since a predetermined reset event; timeout event trigger signal generation means for asserting a timeout event trigger signal when the predetermined control value is at least equal to the number of times the selected one of the plurality of overflow signals has been asserted since a predetermined reset event.

Bailey's figure 8 shows a counter 530 connected by a line 542 to a clock 540. The output of the counter on line 532 is provided to registers 510A 510B and 510C together with comparator circuits 550A, 550B and 550C, which provide outputs to the timeout logic 560 via lines 552A, 552B and 552C. These signals are then used together with the output on line 585 from the timeout logic 560 to determine that a timeout condition has occurred (col. 7, lines 15-35).

Referring to applicant's arguments (see Appeal Brief, page 16), and further in light of figure 4 of the present application, the generation of the timeout signal differs from the Bailey's reference, since Bailey fails to disclose selection

means to receive a plurality of overflow signals and a counter for counting the number of times the selected one of the plurality of overflow signals has been asserted and asserting a timeout event trigger signal based on the overflow signals and the counter value. Therefore the above claim overcomes the Bailey reference.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elmira Mehrmanesh whose telephone number is (571) 272-5531. The examiner can normally be reached on 8-5 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-

direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).